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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,240	09/26/2001	Randhir P.S. Thakur	500996.01	2159

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EXAMINER	
YEVSIKOV, VICTOR V	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,240	THAKUR ET AL.	
	Examiner	Art Unit	
	Victor V Yevsikov	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 38-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,16,18-20,38-45 and 47-50* is/are rejected.

7)☒ Claim(s) *10-15,17,46 and 51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 9, 16, 18 – 20, 38-45 and 47-50 are rejected under 35 U.S.C. 102(e) as being anticipated by Parekh et al. (US 2002/0110975 A1).

With respect to claims 1-5 Parekh teaches a method for forming a transistor, comprising:

a polycrystalline layer 122;

a rough layer formed from an undoped silicon, the rough layer being formed on the polycrystalline layer and including protrusions extending from a surface of the layer (fig. 10; §§ 0010, 0044), and wherein:

2. the protrusions include hemispherical protrusions;

3. the polycrystalline layer comprises a conductive polycrystalline material;

4. the polycrystalline layer comprises a conductive alloy that becomes polycrystalline at a temperature about 560^{O}C;

5. the polycrystalline layer comprises a bottom electrode 122 of a capacitor and wherein the protrusions of the rough layer increase the surface area of the bottom electrode so as to increase the capacitance of the capacitor.

With respect to claims 6-9 Parekh teaches a method for forming capacitor, comprising:

a top electrode 126;

a dielectric 124 coupled to the top electrode; and

a bottom electrode 122 coupled to the dielectric, wherein the bottom electrode protrusions formed from undoped silicon, and wherein the electrode layer is formed from a polycrystalline material (fig. 10; §§ 0010, 0044), and wherein:

7. the electrode layer of the bottom electrode forms an outer surface of the capacitor, and wherein the rough layer forms an inner surface of the capacitor (fig. 11).

8. the bottom electrode 122 comprises an outer surface, an embedded layer, and an inner surface to define a container structure, wherein the rough layer defines the inner surface and the outer surface, and wherein the relatively smooth surface defines the embedded layer (fig.11),

9. the undoped silicon includes undoped amorphous silicon (§ 0045).

With respect to claims 16 and 18-20 Parekh teaches a method for a semiconductor structure, comprising:

forming a polycrystalline layer ; and

forming hemispherical protrusions in an undoped silicon layer that overlies the polycrystalline layer (fig. 10; §§ 0010, 0044), and wherein:

18. forming hemispherical protrusions includes depositing the undoped silicon layer by using low-pressure chemical vapor deposition of silane gas at a temperature less than about 550 degrees Celsius and greater than about 450 degrees Celsius (§ 0045),

19. forming hemispherical protrusions includes forming atomic seeds from which hemispherical protrusions are grown by chemical vapor deposition of silane gas at a temperature less than about 600 degrees Celsius and greater than about 550 degrees Celsius (§ 0045),

20. forming hemispherical protrusions includes annealing so as to grow the atomic seeds to form hemispherical protrusions (§ 0045).

With respect to claims 38-41 Parekh teaches a method for forming a semiconductor structure, comprising:

a first layer formed from an undoped substance and including first and second surfaces, the first surface including a plurality of surface protrusions that increase a surface area of the first layer; and

a second layer formed abutting the second surface of the first layer and including a plurality of atoms, the atoms in the second layer being sufficiently bound in the second layer to substantially remain in the second layer during formation of the first layer (fig. 11; §§ 0043,0044); and wherein:

39. the first layer comprises an undoped silicon layer.

40. the undoped silicon layer comprises an undoped amorphous silicon layer.

41. the second layer comprises a polycrystalline layer.

With respect to claims 42-45 Parekh teaches a method for forming a capacitor, comprising:

a first electrode layer having first and second surfaces formed from undoped silicon,

first and second rough layers formed on the first and second surfaces of the first electrode layer, respectively, each of the first and second rough layers including a plurality of surface protrusions that increase a corresponding surface area of the layer;

a dielectric layer formed on the first and second HSG layers; and

a second electrode layer formed on the dielectric layer (figs. 1, 11; §§ 0002-0009, 0043, 0044); and wherein:

43. the first electrode layer comprises a polycrystalline layer.

44. the first and second rough layers comprise first and second HSG layers,

45. the first rough layer is formed over substantially the entire first surface of the first electrode layer and wherein the second rough layer comprises a segment formed on a first portion of the second surface of the first electrode layer and another segment formed on a second portion of the second surface of the first electrode layer,

With respect to claims 47-50 Parekh teaches a method for forming a semiconductor structure, comprising:

a first electrode layer having first and second surfaces formed from undoped silicon,

a rough layer formed on the first surface of the first electrode layer, the rough layer including a plurality of surface protrusions that increase a corresponding surface area of the layer;

a dielectric layer formed on the rough layer and on the second surface of the first electrode layer, and

a second electrode layer formed on the dielectric layer (figs. 1, 11; §§ 0002-0009, 0043, 0044), and wherein:

48. the first electrode layer comprised a polycrystalline layer,

49. the first and second rough layers comprise first and second HSG layers, respectively.

50. the dielectric layer comprises a first segment formed on a first portion of the second surface of the first electrode layer and a second segment formed on a second portion of the second surface of the first electrode layer.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because not showing each feature claimed.

Object to drawings as semiconductor structure 800 and semiconductor structure 900 will are never depicted as being in the same embodiment

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the terms "first capacitor" and "second capacitor" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

The claims 11-15 are objected to because of the following informalities: As this embodiment was presented in the original claims Applicant can clarify the specification of this embodiment without including new subject matter.

Appropriate correction is required.

Claims 10, 17, 51 and 46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor Yevsikov whose telephone number is (571) 272-1910. The examiner can normally be reached on Monday –Thursdays 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or processing is assigned is (703) 873-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information

for unpublished application is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

V. Yevsikov

Victor Yevsikov
Examiner
Art Unit 2825

December 11, 2004

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
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